Design of a Dynamic Reactive Power Compensator (DRPC) to Improve the Power Factor of a Load Center

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Abstract: Power systems loads are very dynamic. Varying reactive power causes voltage fluctuation, line overloading, increase power transmission loss and voltage instability. To minimize these effects, the network operators charge for kVA demand, which forces the customers to reduce the reactive power consumption. This paper discusses about the Dynamic Reactive Power Compensator (DRPC) as one of the FACTS device technology. Continuous and smooth reactive power compensation will improve the power system performance. This brings down voltage fluctuation, power loss in the transmission system and threat on instability while reducing the kVA demand charges. Further the transmission lines can be utilized to transmit more active power while improving the reliability of the supply. A control system for DRPC has been developed; simulated using EMTDC/PSCAD and results are provided in the paper. This paper presents a complete preliminary simulation study of a DRPC controller.

Keywords: Reactive power, power system, kVA demand and FACTS devices

1. Introduction

Increasing population and industrialization created a dramatic increase in the electrical energy demand. Most of the industries consume large amount of reactive power mainly due to the large and medium size rotating machines [1, 2]. The reactive power consumption reduces the power factor of the load center. This reduces the power transfer capability of the transmission lines while causing under voltage problems [1]. Introduction of power electronic applications to power system effectively involves in regulating voltage, in mitigating voltage flickers and in improving power factor [2]. Researchers have proposed the usage of FACTS devices to increase the power transfer capability of transmission networks and to have direct control of power flow in the lines [3]. Reactive power compensation improves the power system performance in many ways such as improving the power factor, boosting the voltage, enhancing the power transfer capability, controlling the power oscillations and improving the system stability [4-6]. Correct choice of power electronic devices and its control is thus mandatory to achieve effective and efficient performance.

There are different variety of FACTS devices developed to increase the power system performances [5, 6]. Static VAr Compensator (SVC) is used as one of the shunt connected type FACTS device to improve the power system performance.

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Initially SVCs were developed to compensate for the fluctuating industrial loads such as arc furnaces. Later researchers found that a SVC can be used for various purposes such as reactive power compensator, voltage booster and power fluctuation damper [7].

Fixed and switched capacitors are used very often in power system to enhance the system voltage profile [8]. It was noted that Breaker Switched Capacitor/ Thyristor Control Reactor (BSC/TCR) based reactive power compensator reacts quickly to a disturbance than mechanically switched type [2].

This paper discusses VAr Compensation Using a Flexible Alternative Current Transmission System (FACTS) Device named as Dynamic Reactive Power Compensator (DRPC). This is the first study in Sri Lanka carried out to develop and implement a DRPC.

The proposed system is modeled using the EMTDC/PSCAD program in the time domain [Annex 1]. Simulation results are listed and suitability of the DRPC system is discussed.

2. Materials and Methods

The feasibility of the proposed system was studied at the Faculty of Engineering, University of Peradeniya. The aim of this study is to maintain the power factor of the load center of the faculty closer to unity as seen from the utility side.

The Faculty of Engineering has many laboratories, consisting of several rotating machines with large inertia. Most of these machines are induction type. Therefore the faculty itself consumes a considerably large amount of reactive power from the utility to run these types of inductive loads. This study was mainly focused on to compensate the reactive power consumption. The study had several steps as listed below. (i) power flow measurement carried out at the Faculty transformer, (ii) model the system, (iii) development of control system for the DRPC, (iv) selection of components for the DRPC and (v) simulation study using EMTDC/PSCAD

3. Power Flow Measurements

University of Peradeniya is supplied electricity through an underground 11 kV ring network laid around the university as shown in Figure 1.

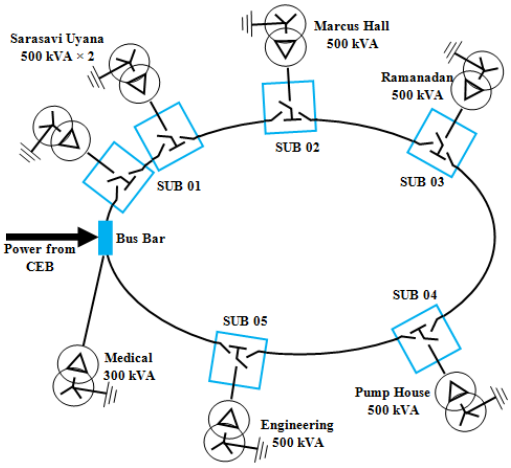


Figure 1: 11 kV underground ring network of the University of Peradeniya

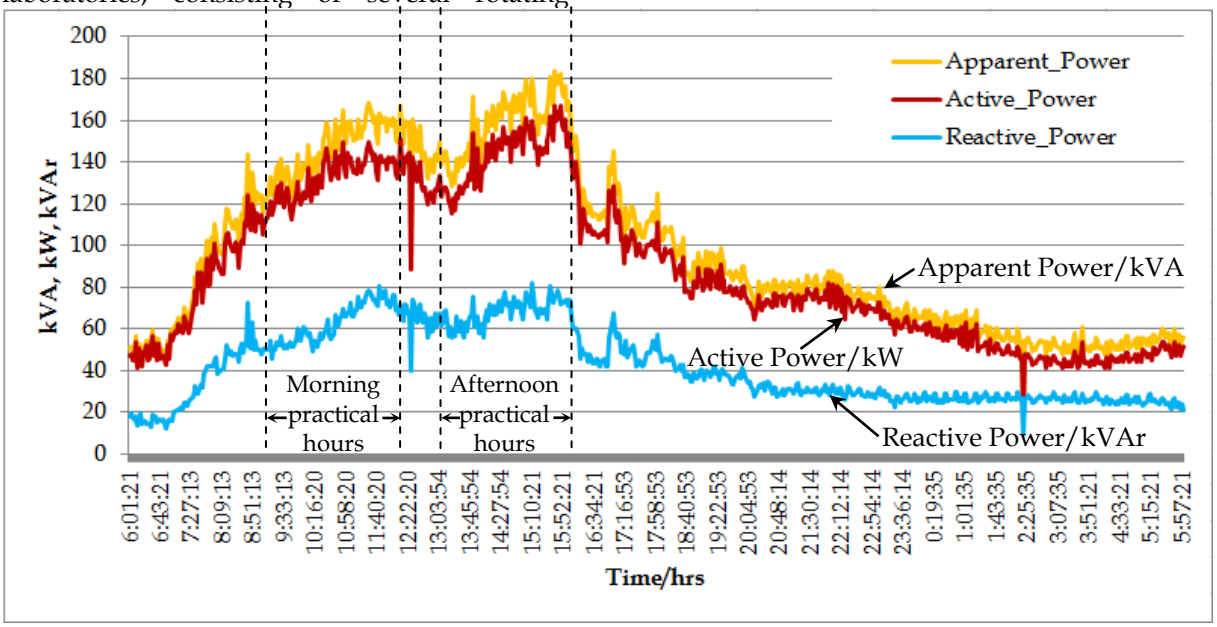


Figure 2: Total power flow measured at the faculty transformer

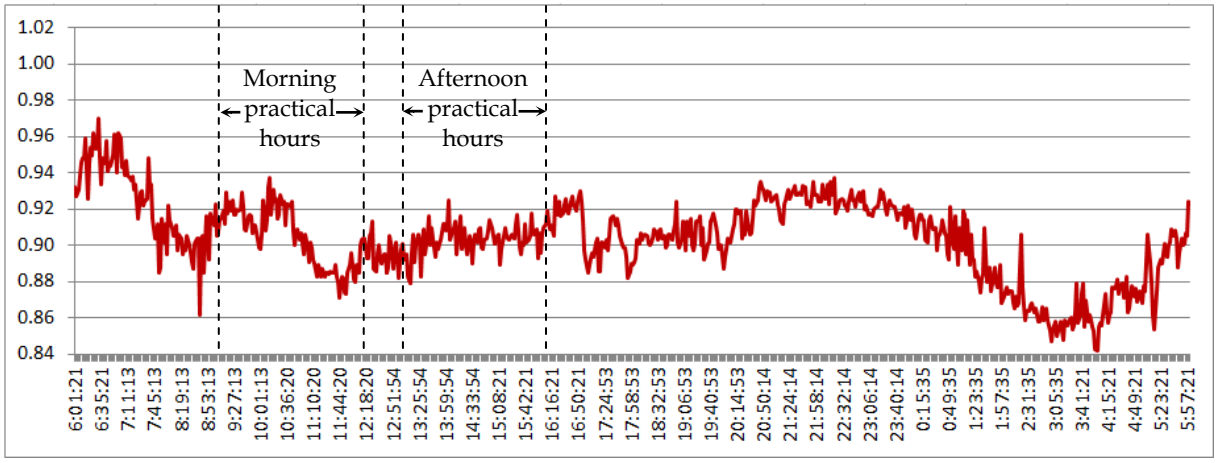


Figure 3: Power factor observed at the faculty transformer

Faculty of Engineering and Akbar-Nell hall are supplied through the transformer placed at the Faculty of Engineering (SUB 05 in Figure 1). Since these are supplied by two different low voltage feeders, the power flow measurements were taken separately for a full day using YOKOGAWA power data logger (CW 150). Figure 2 shows the total power flows from the two feeders of the Engineering faculty transformer. In the Engineering faculty mostly the practical sessions are scheduled 09.00 hrs – 12.00 hrs in the morning and 13.00 hrs – 16.00 hrs in the evening. During this time a number of electrical machines are used. Power flow measurement clearly shows that Engineering faculty consumes a peak reactive load of 85 kVAr. This peak reactive load consumptions can be observed twice a day, falling in the morning "10.30 a.m. – 11.30 a.m." and in the evening "2.30 p.m. – 3.30 p.m.". Engineering faculty consumes an average reactive power of 50 kVAr.

Figure 3 shows the power factor variation of the load seen at the faculty transformer. Load power factor is varying in the range between 0.84 and 0.97 and an average power factor 0.90 was observed from averaging the observed instantaneous power factor.

4. Proposed Control Technique

The DPRC controller is discussed in two sections namely (i) system level controller and the (ii) device level controller. Figure 4 shows the block diagram of the simulated DRPC controller model. Figure 5 shows the circuit diagram of the DPRC, which includes single phase BSC and TCR Circuit.

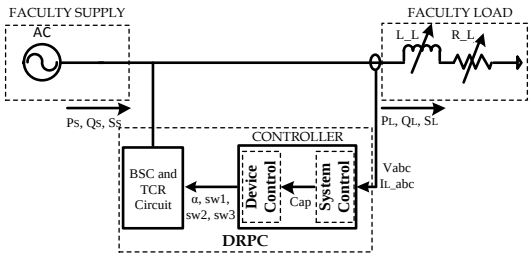


Figure 4: Simulated model of DRPC

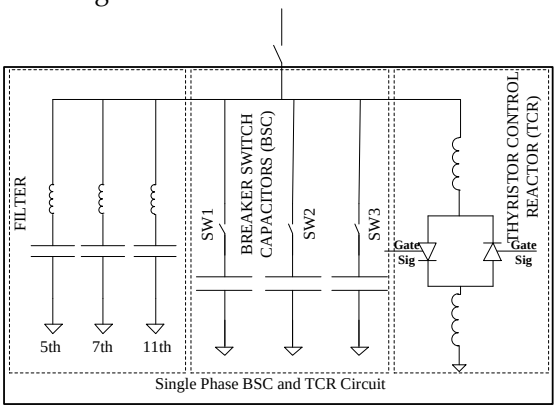


Figure 5: Single Phase BSC and TCR Circuit

A resonance filter was designed to remove the 5th, 7th and 11th harmonics introduced by the thyristor switching operations. Further, the filter is capable of supplying the constant reactive power demand, which is about 50 kVAr at this load centre.

4.1. System Level Control

Three phase voltage vector Phase Locked Loop (PLL) was used to track the system frequency angle theta (θ) [9]. Locally measured three phase voltages were transformed to d-q frame using the transformation matrix shown in equation 1.

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \frac{2}{3}\begin{pmatrix} Cos\theta & Cos(\theta - 2\pi/3) & Cos(\theta + 2\pi/3) \\ -Sin\theta & -Sin(\theta - 2\pi/3) & -Sin(\theta + 2\pi/3) \end{pmatrix}\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (1)$$

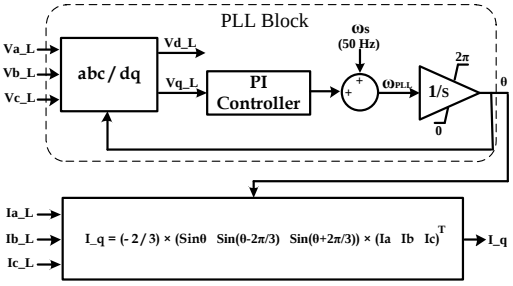
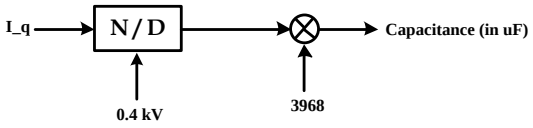


Figure 6: Control block diagram of the PLL and d-q transformation

Figure 6 shows the block diagram of PLL with the d-q transformation block. At the steady state the magnitude of Vq_L becomes zero. In case of a disturbance, Vq_L gets a nonzero value. The PI controller regulates the Vq_L to zero thus tracks the system frequency. This is done by adjusting the PLL frequency (ω_{PLL}) according to the PI controller output.

Further in the controller model d-q transformation was used to find the Quadrature-Phase component of the load currents (Iq_L) [Annex 4].



$$\left(\frac{\sqrt{3}}{\sqrt{2}}\right) \times \left(\frac{10^6}{2 \times \pi \times 50}\right) = 3968$$

Figure 7: Controller to find the capacitance

Figure 7 shows the controller (feed forward action), which uses q-component of the line current to find the capacitor value. The controller uses locally measured load currents and reference voltages to calculate the reactive power drawn by load center. The calculated reactive power is injected by adjusting the impedance of the DRPC according to the output of the device control.

4.2. Device Level Control

reakers of the BSCs and TCR were controlled according to the reactive power demand beyond the flat demand. Figure 8 shows the control block to switch the breakers of the BSCs. Depend on the reactive power demand the breaker switches are operated to supply the reactive power to the load.

Thyristor firing angles were controlled to vary smoothly the reactive power supplied by DRPC. When a BSC is switched on the TCR is set to its maximum to compensate for the BSC. When the reactive power demand increases the firing angle is increased, which reduces the TCR contribution and thus allow supplying the demand from DRPC. Figure 9 shows the control block for the thyristor switching angle.

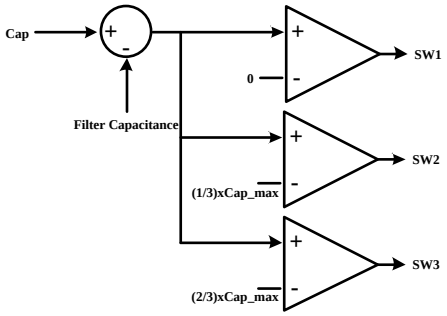


Figure 8: Breaker control of the BSCs

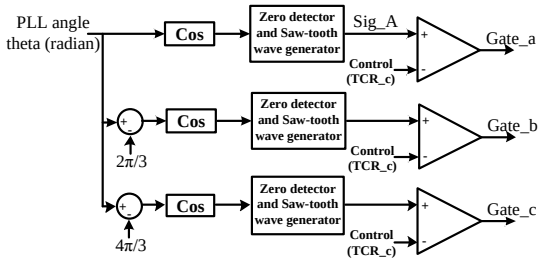


Figure 9: Thyristor firing angle control

5. Selection of Circuit Parameters

From the measurements taken at the Faculty transformer, it was observed that Engineering Faculty consumes a peak reactive load of 85 kVAr. Furthermore it was noted that the minimum reactive power consumption was about 20 kVAr. Therefore the design was focused to supply a fixed reactive power of 20 kVAr and a maximum of 90 kVAr. The fixed compensation was supplied by the filter capacitors. Rest of the variable reactive power compensation was done by controlling the BSCs together with the TCRs. Filter capacitor values were calculated to supply the fixed reactive power and the filter inductor values were calculated to filter the mentioned harmonics. BSC values were calculated to compensate for the demand Q beyond the fixed compensation and the TCR inductor value was calculated to compensate for the one of the three equal BSCs. For the capacitor value calculation equation 2 was used.

$$Q = \frac{V^2}{\omega C} \quad \rightarrow \quad C = \frac{V^2}{Q\omega} \qquad (2)$$

Equation 3 was used to calculate the filter inductor values.

$$n\omega L = \frac{1}{n\omega C} \rightarrow L = \frac{1}{(n\omega)^2 C} \quad (3)$$

Where n- harmonic number

TCR value calculation was done using equation 4. Two inductors of similar values were used in the both sides of the thyristor switches. Table 1 shows the calculated component values for per phase.

$$\omega(2L) = \frac{1}{\omega C} \rightarrow L = \frac{1}{2C(\omega^2)} \quad (4)$$

Table 1: Per phase Component Values

Category	Capacitance/uF	Inductance/mH		
Filter	3Nos × 134	Harmonics Arms		
		5th	7th	11th
		3.03	1.54	0.63
BSC	3Nos × 510	-		
TCR	-	2Nos × 9.93		

6. Simulation Results

A Dynamic Reactive Power Compensator model was developed using EMTDC/PSCAD tool, which is shown in Figure 4. The simulated DRPC uses BSC and TRC to compensate for the reactive power demand. Filters were modeled to eliminate the 5th, 7th and 11th harmonic components. The Engineering Faculty transformer and the upstream network were modeled as an AC voltage source with impedance. The loads were modeled using variable resistor and variable reactors.

The study was done with introducing load variation exactly same to the measured data obtained at the Engineering Faculty transformer. Considering the running time and the limited computer performances, simulation was done in a compressed time span. The measured load data file was imported into the PSCAD simulation. Selected 1000 data points with 2 minutes time interval were imported to get the exact power variation as shown in Figure 2 [Annex 2]. When the data were imported to the PSCAD, the total one day period of measurement were compressed to run within 12.0 seconds (2 hrs. ≡ 1.0 second). By referring to the imported measured data the resistance and inductance were calculated based on P and Q [Annex 3].

In the controller model d-q transformation was used to find the in-phase and the quadrature-phase components of the line currents. Variable capacitors were used as the reactive power compensators. A dynamic controller, which uses the q-component of the line current, was developed to find the capacitance of the variable capacitor. Figure 10 and 11 shows the load variation and the power factor variation respectively in simulation model.

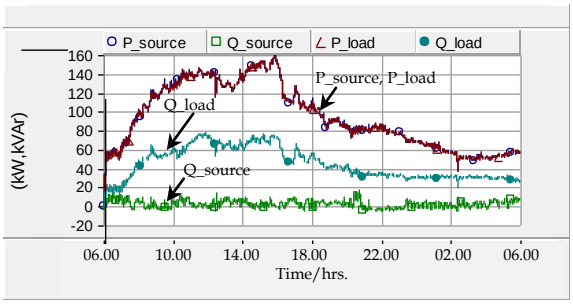


Figure 10: Load variation obtained from simulation

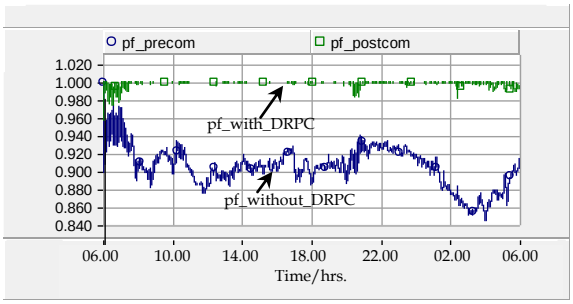


Figure 11: Power factor variation obtained from simulation

The load power variation and power factor variation (pf_without_DRPC) obtained from simulation are matched with the measured information. This confirmed that the load model is correctly developed in the simulation.

The reactive power consumed from the source is shown as zero. This confirmed correct functioning of the control developed for the DRPC.

The real power demand exactly matches the real power supplied by the AC source. This confirms the total reactive power consumed by the load is supplied by the DRPC.

Figure 11 depicts the power factor variation before and after engaging the DRPC to the system. This confirms that the proposed DRPC improves the power factor towards unity.

Figure 12 shows the BSC switching signal generation according to the calculated capacitance variation [Annex 5]. Depend on the reactive power requirement one or two or all three BSCs were switched on to supply the reactive power to the load. Figure 13 shows the simulation results of the TCR control signal for

phase-A. Where theta comes from PLL and the Sig_A shows the saw-tooth wave form [Annex 6, 7]. Comparison of saw-tooth wave and the TCR control signal the firing pulses were generated as shown in the Figure 12.

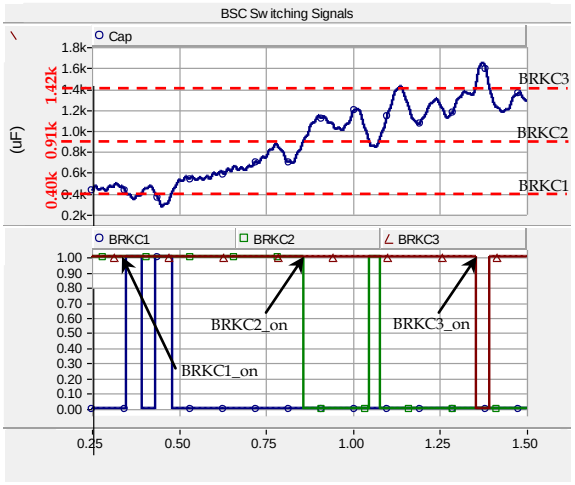


Figure 12: BSC switching signal generation

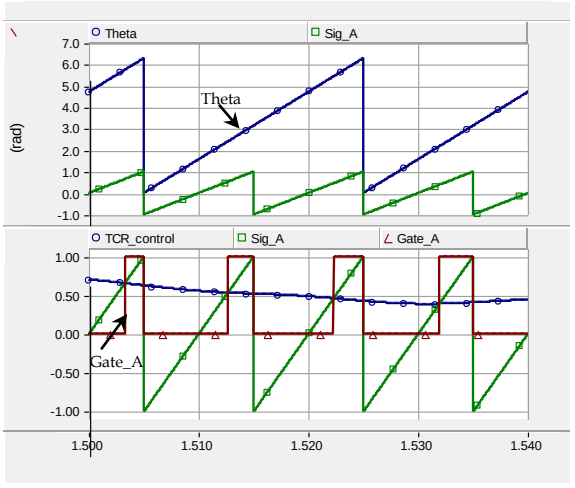


Figure 13: TCR control and gate signals

Figure 14 shows the simulation results with BSCs-TCR based DRPC. Simulation results clearly shows that the calculated current by the controller (Ia_injected) exactly match with the shunt injected current measured (Ia_measured) in the PSCAD simulation.

Lagging phase shift between the voltage (Va_load) and current (Ia_load), indicates the reactive load at the load center. The current coming out from the source (Ia_source) is in-phase with the voltage. This confirms the load is seen as purely resistive by the source. Furthermore the transformed q-component (I_q_s) of the source current is kept at zero. This makes sure the reactive power drawn from the AC source is zero.

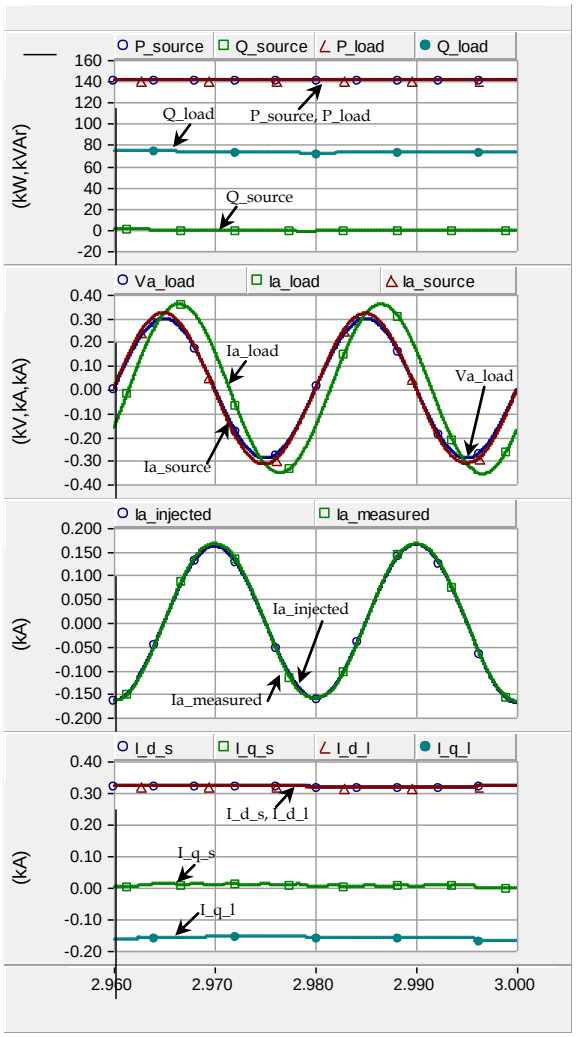


Figure 14: The simulation results at 2.96 – 3.00 s

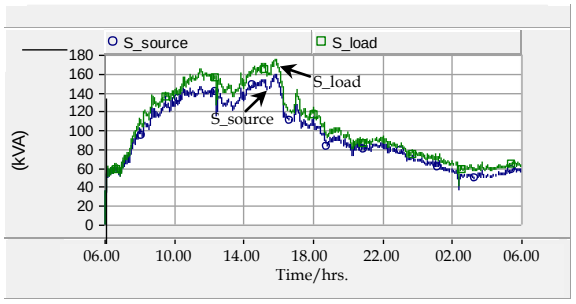


Figure 15: Apparent power comparison

Figure 15 shows the kVA demand of the load and supply. This proves that the peak kVA demand reduced nearly from 180 to 160. Thus in terms of electricity bill reduction (with the current kVA demand charge of 850 rupees [10]), is 17000 rupees per month. In addition to this the stress on the 11 kV ring network also reduced.

When this is implemented and extended to the whole university electricity distribution system, the kVA demand reduction will reduce the electricity bill drastically. As a result the money saved will payback of the cost of implementation. Further this study and

endurance will boost further application of DRPC, built locally under proper guidance and customization to user demands, so that CEB can apply this modern application to boost the voltage profile at the load centers where applicable.

7. Conclusion

Simulation results confirm that the reactive power drawn from the source is kept at zero by the controlled DRPC injection. Addition to the power factor improvement, always a reactive power compensator boosts the bus bar voltage. Since the kVA charges are high, reduction in kVA demand will reduce the electricity bill by a considerable amount. More to this peak shaving of the kVA demand helps the utility to supply power with comparatively less line losses.

This research will give a motivation to implement DRPC locally made in Sri Lanka with low cost. This DRPC can be used for power quality improvement in the city area, where low voltage problems are being addressed. Furthermore this can be used to enhance the power transfer capability of the lines. Therefore the distribution lines can be extended effectively to electrify the rural areas of the country.

Acknowledgement

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Future Plans

This study can be extended to compensate the reactive power in all over the country, thus a flat voltage profile can be achieved. By changing the control action this DRPC can be used to improve power system performances in different ways such as power fluctuation damper and voltage booster.

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Annex 1

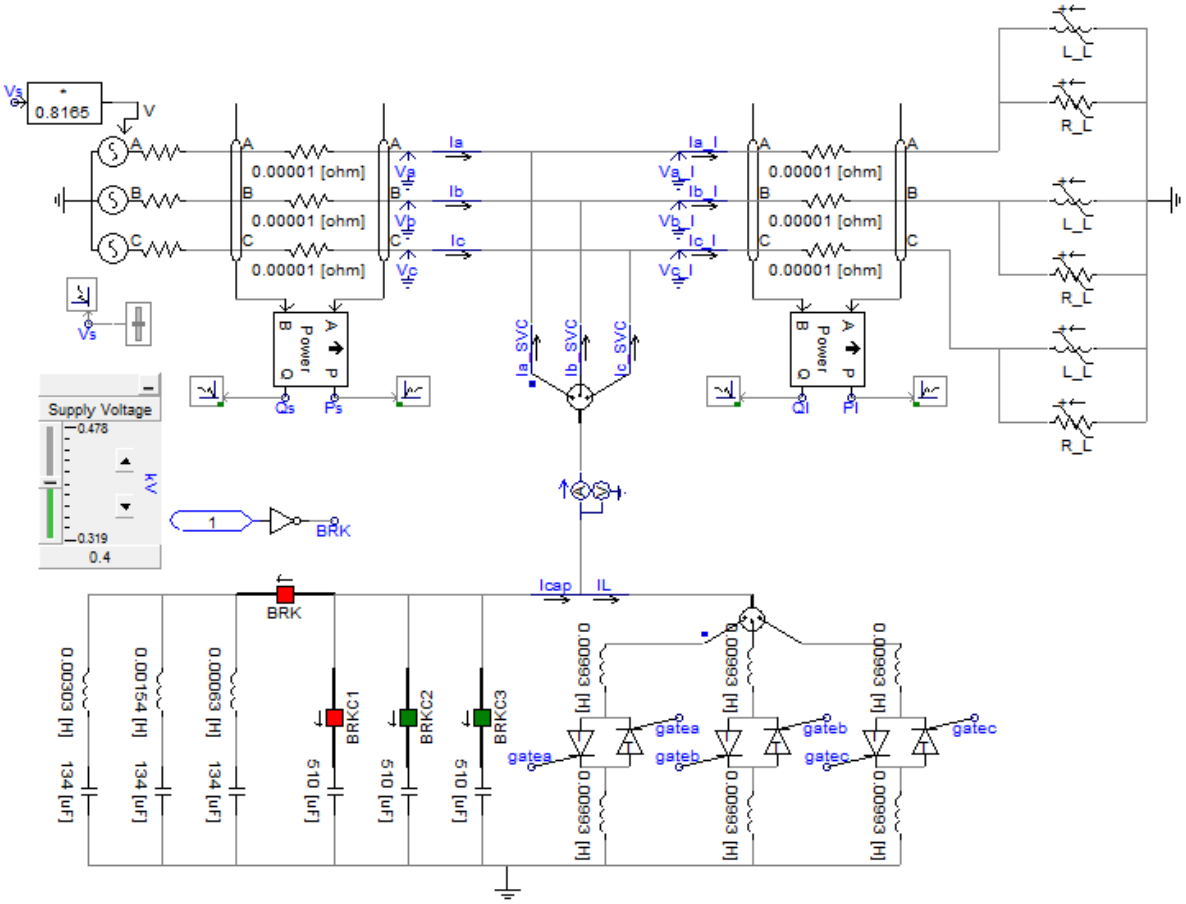

Figure 16: PSCAD model developed for DRPC simulation

Annex 2

Measured load data at the Faculty transformer was imported to PSCAD using the data file importer available in the PSCAD library. Figure 16 shows the data file arrangement for importing measured "P" and "Q" data

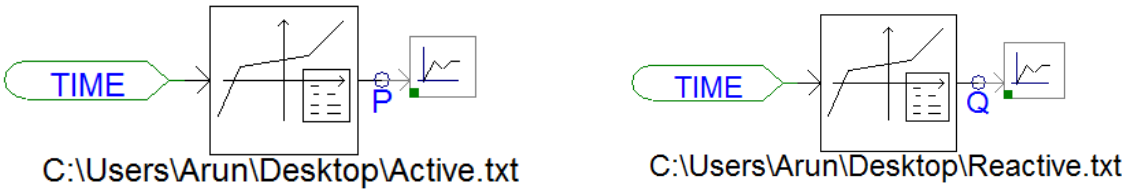

Figure 17: Data file importer

Annex 3

Exact load variation was obtained by calculating the load resistance and reactance based on the imported data. Figure 17 shows the simulation blocks used to calculate the loads.

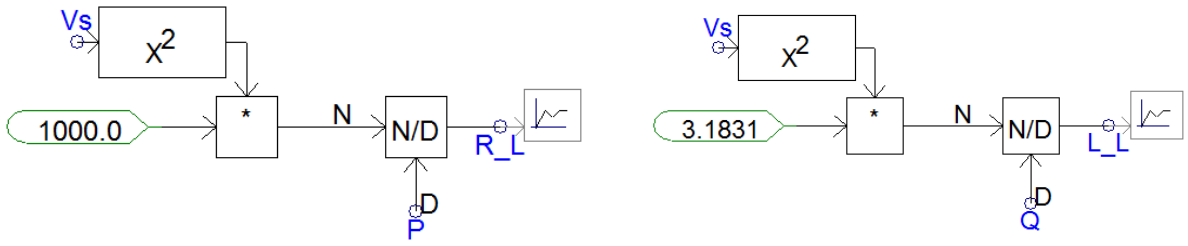

Figure 18: Load Calculation

Annex 4

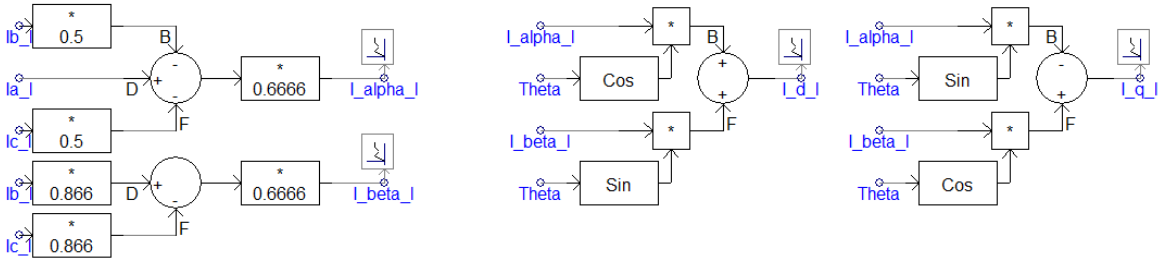

Figure 19: d - q transformation

Annex 5

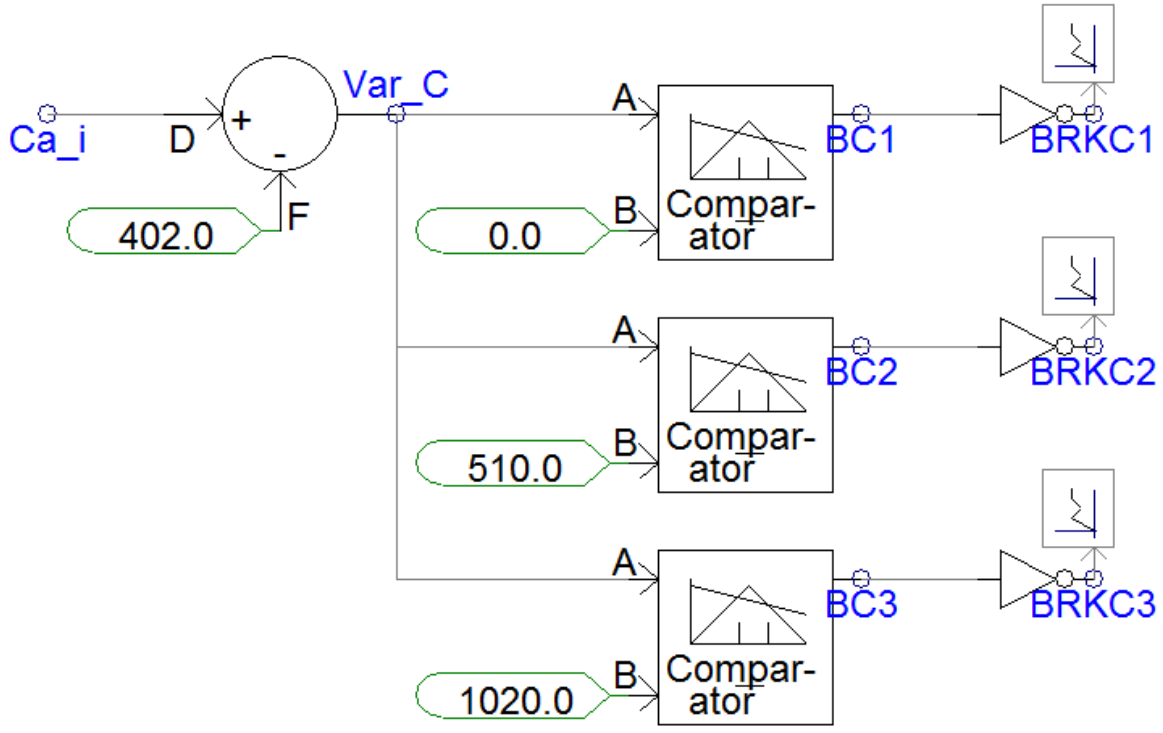

Figure 20: BSC switching signals

Annex 6

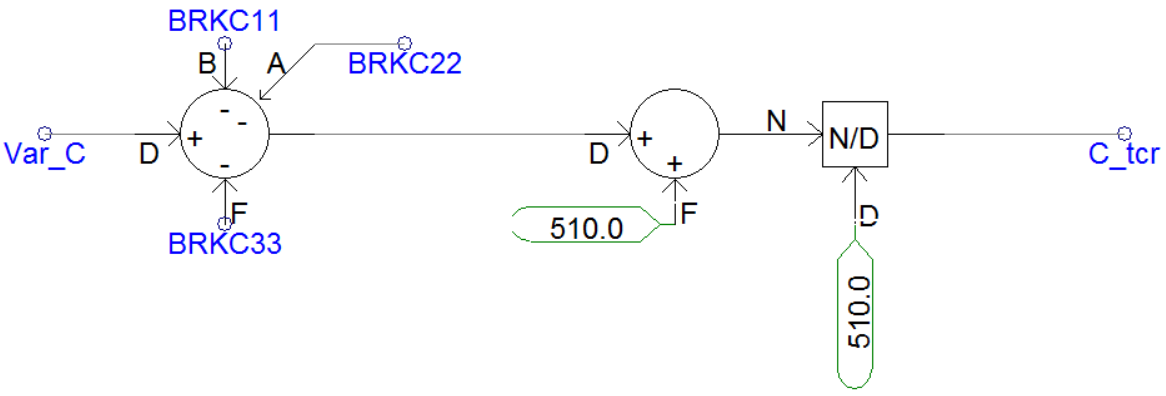

Figure 21: Thyristor control signal generation

Annex 7

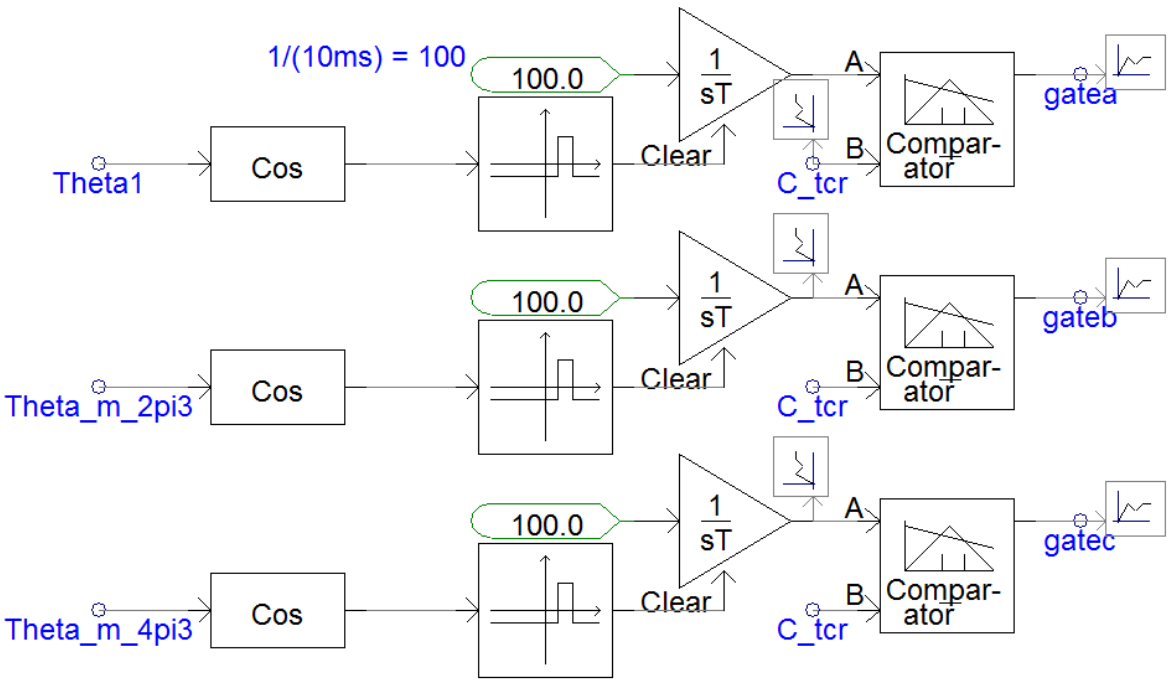

Figure 22: Gate signal generation