



Mechanical exfoliation of graphene from Sri Lankan vein graphite for field effect transistor application

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Abstract

Graphene is one of the most promising nanomaterial due to its unique combination of exceptional properties with wide range of applications. Single atomic thickness with extremely high electron mobility and a zero-band gap provides many advantages to the graphene as an electronic material. Sri Lanka is one of the countries having a vein graphite with high purity of carbon. However, Sri Lanka is still exporting the graphite as a raw material.

This research was carried out to exfoliate mono layer graphene from Sri Lankan vein graphite and to fabricate field effect transistors and to study electronic properties. We used a simple scotch tape technique to transfer single layer of graphene onto a 300 nm $\rm SiO_2$ coated Si substrate. The graphene sheets which are produced using this method have been given a high quality, incomparable with other methods with lateral sizes up to $100\mu m$. The thickness and the uniformity of the graphene layer were tested using Atomic Force Microscopy (AFM). The thickness was confirmed to be 0.4 nm as shown in the Figure. The AFM images also confirmed the presence of double layer graphene with thickness of 0.9 nm. The Field Effect Transistor was fabricated by making electrical contact using thermal evaporation of gold and we found that the graphene layer showed an ambipolar current response with a positive Dirac voltage. Also, we calculated the electron and hole mobility in the graphene channel. Electron mobility of the FETs was smaller than the hole mobility which indicates the increase effective mass of electrons in Sri Lankan graphene Our studies suggested that the Sri Lankan graphite is one of best raw material for graphene exfoliation and the graphene exfoliated can be used for device applications.

Keywords: Graphene; Graphite; Sri Lanka Graphite; Field effect transistor; mobility

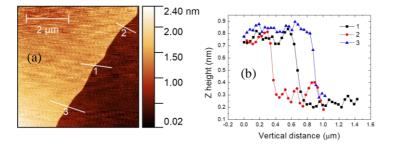


Figure: (a) AFM image of the transferred graphene film on the Si/SiO2 substrate and (b) the surface profile across the lines named as 1, 2 and 3